

## REMARKS

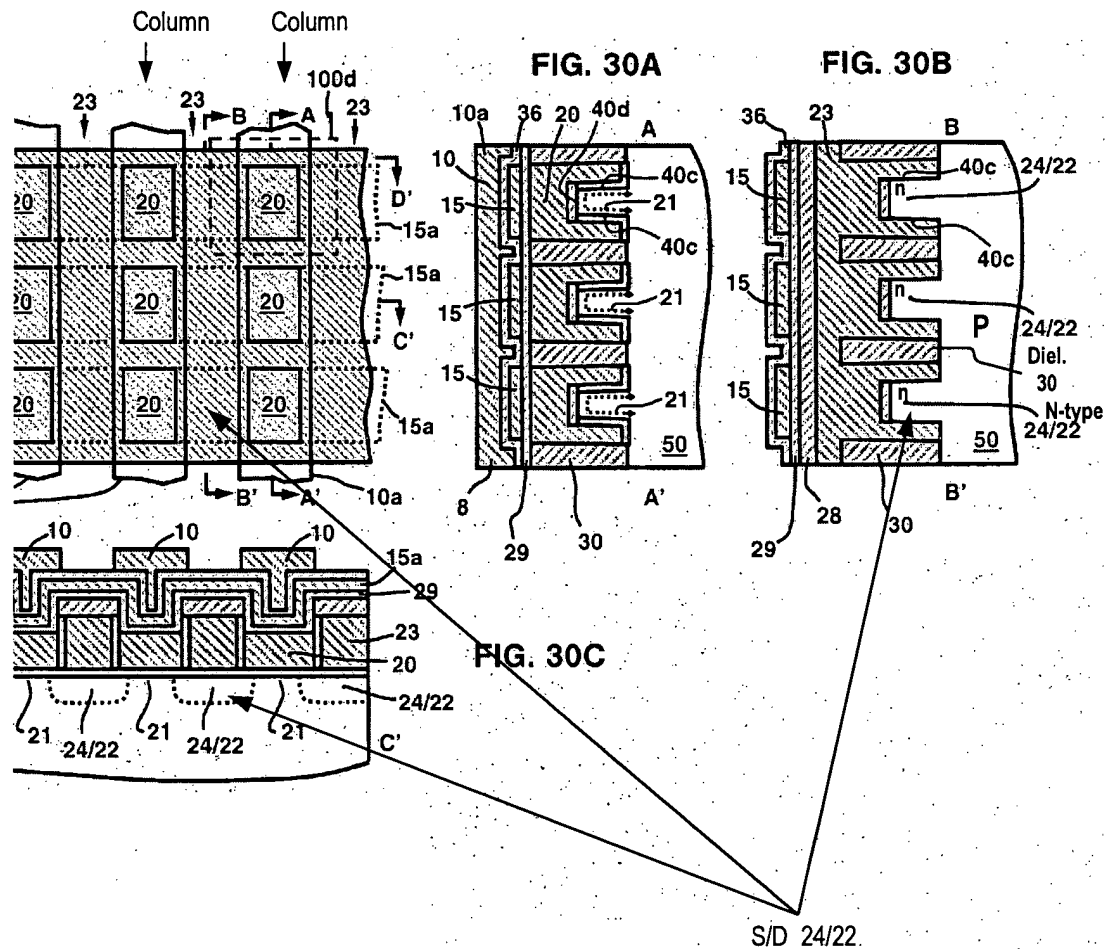
Claims 1-14 were rejected under 35 U.S.C. 103(a) over Applicant's prior art Figures 1-8 in view of Wang (US 2004/0004863 A1).

Claim 1 recites:

wherein in each column of the array, for any two consecutive memory cells, one source/drain region of one of the cells and one source/drain region of the other one of the cells are provided by a contiguous region of the first conductivity type in the semiconductor substrate, each contiguous region providing source/drain regions to only **two of the memory cells in said column** ...

This recitation is supported by Applicant's specification, page 4, lines 5-10. The contiguous regions read on regions 174. Claim 1 is not limited to the embodiments discussed herein, however.

The Examiner states that Applicant's contiguous regions are disclosed in Wang's Figures 30-31, pages 16-17, paragraphs [0115]-[0118]. This is incorrect. A column cross section along a bitline 23 is shown in Wang's Fig. 30B and reproduced in a diagram below. Source/drain regions 24/22 are n-type regions formed in p-type substrate 50. See paragraph [0045], lines 4-6 ("substrate 50 ... p-type ..."); and the last nine lines of paragraph [0045] ("regions 24/22 ... n-type ..."). In Fig. 30B, each n-type region 24/22 provides a source/drain region to only one memory cell in a given column, even though each region 24/22 provides source/drain regions to two memory cells in two adjacent columns (Fig. 30C). The following diagram marks one source/drain region 24/22 in Figs. 30, 30B, 30C:



In the view of Fig. 30B, n-type regions 24/22 do not meet together due to the presence of dielectric 30 (marked in diagram below and in Wang's Fig. 16A). Note paragraphs [0045] and [0048] describing how the regions 24/22 are doped. Therefore, each contiguous region 24/22 provides a source/drain region to only one memory cell in a given column. Further, even assuming for the sake of argument that the adjacent n-type regions 24/22 would meet together to form a combined contiguous region extending along the entire column, the combined contiguous region would provide source/drain regions to all the three memory cells in the column, not "only two of the cells" as recited in Claim 1.

**Claim 2** depends from Claim 1.

**Claim 3** depends from Claim 2, and further recites that the source/drain regions of one of the columns are separated from the source/drain regions of another one of the columns by field isolation regions in the semiconductor substrate.

In Wang's Fig. 30C, the source/drain regions 24/22 of different columns are separated by channel regions 21 and not by field isolation regions as in Claim 3.

**Claims 4-6** depend from Claim 1.

**Claims 8-14** are believed to be allowable for reasons similar to the reasons given above for the respective Claims 1-7.

New Claim 15 is supported by Applicant's Figs. 10A, 10B and the specification paragraph [0022] (pages 4-5). Each memory cell has an active area which is part of the array's active area 222. The active areas 222 of each column are separated by field dielectric regions 220. Each region 220 fills a trench 220T running through the array in the column direction (X-direction).

Claim 15 is not limited to the embodiments discussed herein.

In Wang's Fig. 30C, the source/drain regions 24/22 and the channel regions 21 of different columns are not separated by a dielectric region as in Claim 15.

Claim 16 depends from Claim 15.

Claim 17 is supported by Applicant's Fig. 31A, showing two channel regions. Each channel region extends between adjacent source/drain regions 174 in the column direction (X direction, i.e. the direction of bitline 180).

Claim 17 is not limited to the embodiments discussed herein.

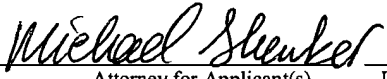
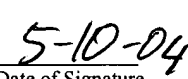
In Wang's Fig. 30C, each channel region 21 extends in the row direction, not the column direction as in Claim 17.

Claim 18 depends from Claim 17. Claim 18 is supported by the last three lines of paragraph [0043] (pages 7-8), but is not limited to the embodiment described therein.

Claims 19-22 are believed to be allowable for reasons similar to the reasons given above for the respective Claims 15-18.

Claims 23-26 and 27-30 are believed to be allowable for similar reasons.

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 10, 2004.	
 Attorney for Applicant(s)	 Date of Signature

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